What is claimed is:

(1) A bond out chip comprising:

a first chip; and

a plurality of input/output pads which are disposed on at least second chip adjacent to said first chip and which are communicatively coupled to said first chip.

(2) The bond out chip of claim 1 wherein said first chip and said at least one second chip are spaced apart and are separated by at least one scribe line.

(3) The bond out chip of claim 1 wherein said first chip is substantially identical in architecture to a production chip with the exception of a connection layer.

(4) The bond out chip of claim 3 wherein at least one second chip is substantially identical in architecture to said first chip, with the exception of a connection layer.

(5) The bond out chip of claim 4 wherein said first chip and said at least one second chip are formed on a semiconductor wafer.

(6) The bond out chip of claim 5 wherein said wafer has plurality of reticle zones, and said first chip and said at least one second chip each reside within the same reticle zone.

(7) The bond out chip of claim 2 wherein said first chip includes an active core portion and said at least one second chip includes a disabled core portion.

(8) The bond out chip of claim 7 wherein said disabled core portion is disabled by use of a at least one connection layer, said active core portion is activated by use of said at least one connection layer, and said plurality of input/output pads are communicatively coupled to said first chip by use of an interconnection layer which is disposed above said at least one connection layer and which traverses said at least one scribe line.

(9) The bond out chip of claim 1 wherein said at least one second chip further comprises a plurality of input/output buffers which are communicatively coupled to said first chip.

(10) The bond out chip of claim 1 wherein said first chip comprises a microcontroller.

(11) A bond out chip formed on a semiconductor wafer comprising:

a first chip having an active core portion and which is substantially identical in architecture to a production chip with the exception of at least one connection layer;

and

an adjacent chip which is substantially identical in architecture to said first chip with the exception of said at least one connection layer, which is spaced apart from said first chip and separated from said first chip by a scribe line, and which includes a disabled core portion and a plurality of input/output buffers and pads which are communicatively coupled to said first chip across said scribe line and which are adapted to allow said first chip to be coupled to an in-circuit emulator.

(12) The bond out chip of claim 11 wherein said first chip further includes a plurality of drivers for communicating with said in-circuit emulator, and which are communicatively coupled to said plurality of input/output buffers and pads.

(13) The bond out chip of claim 12 further comprising a connection layer for activating said plurality of drivers and communicatively coupling said input/output buffers and pads to said first chip.

(14) The bond out chip of claim 13 wherein said first chip comprises a microcontroller.

(15) A method of manufacturing a bond out chip, comprising

the steps of:

forming a plurality of spaced apart chips on a semiconductor wafer each having a core portion and input/output pads;

activating the core portion of a first chip;

disabling the core portion of at least one second chip which is adjacent to said first chip;

connecting said first chip to the input/output pads of said at least one second chip; and

removing said first chip and second chip together from said wafer, thereby forming a bond out chip.

(16) The method of claim 15 wherein the steps of activating the core portion of a first chip and disabling the core portion of at least one second chip are performed by forming a connection layer for said first chip and said at least one second chip.

(17) The method of claim 16 wherein the step of connecting said first chip to the input/output pads of the at least one second chip is performed by forming an interconnection layer on top of said connection layer.

(18) The method of claim 16 wherein the step of connecting said first chip to the input/output pads of the at least

one second chip is performed by forming said connection layer.

(19) The method of claim 15 wherein each of said chips is substantially similar in architecture.

(20) The method of claim 19 wherein said chips are separated by scribe lines.